Amendments to the Specification:

Please amend the paragraph on page 3, starting at line 7 as follows:

FIG. 1 illustrates a clock recovery unit in accordance with aspects of the present invention. In the clock recovery unit of FIG. 1, a clock signal, such as a local reference clock signal, or as [[i]]in FIG. 1 an external clock signal 39a is provided to a clock phase generator. As illustrated, the clock phase generator is a lumped delay line 3 formed of a series of lumped delay elements. Taps 4 are taken between each of the lumped delay elements. Each successive tap, therefore, is a signal which is slightly delayed with respect to a signal from the preceding tap. As the signal is a clock signal, each tap has a slightly delayed, or phase-shifted, version of the clock signal.

Please amend the paragraph on page 3, starting at line 26 through page 4, line 4 as follows:

The up/down signals are provided to a counter 37. The counter 37 accumulates up/down signals to form a selector signal 8. The selector signal determines which tap a selector circuit 133 selects for use from the lumped delay line. In addition, the counter, in this instance, counts in a rollover fashion. That is, the counter counts from zero to N-1, with the counter returning to zero when the count reaches N. As will shortly be discussed, [[n]]N is determined so that the range of possible taps from the delay line ranges within one clock period of the reference clock. This provides several benefits, including a reduction in false locking, particularly at harmonics of the

data signal. N is determined by the number of taps equivalent to one clock period of the reference clock.

Please amend the paragraphs on page 8, starting at line 5 and continuing through line 31 as follows:

As illustrated in FIG. 3, two multiplexer units 131 and 133 receive outputs from the tapped delay line 137. As those of skill in the art will recognize, in actual practice differing numbers of multiplexers may be used, but the use of the two multiplexer units in FIG. 3 eases discussion. Thus, a first multiplexer unit 133 receives signals from the output taps of the delayed line. A first signal is obtained from the beginning of the delay line, the signal for convenience being termed the zero delay signal. A second signal is also tapped from the delay line, with the position of the second signal being variable. For convenience the second signal is termed the nth delay signal. The zero delay signal and the nth delay signal are provided to a phase detector 35. The phase detector compares the signals and if the signals are out of phase, generates an increment/decrement signal to command increasing or decreasing phase shift of the nth delay signal. In one embodiment, the increment/decrement signal is provided to a counter (not shown) or other circuit element, with the counter or other circuit element providing indication of the difference between the tap of the zero delay and the [[nth]]Nth delay signal, as well as the selector signal(s) for the first multiplexer unit 133.

The phase detector therefore causes the zero delay signal and the [[nth]]Nth delay signal to be in phase. The number of delay taps between the zero delay tap and the nth delay tap provides an indication of the clock signal provided to the tapped delay line.

Please amend the paragraphs starting on page 9, line 5 and continuing through page 10, line 10 as follows:

A second multiplexer unit 131 also receives outputs from the taps of the delayed line 137. The second multiplexer selects a kth delay signal from the delay line and produces the kth delay signal to a second phase detector 31. The second phase detector also receives data from a first data channel 301. If the signals are out of phase, the second phase detector generates the command to change the selection signal to adjust k, i.e., select a different output tap to generate the kth clock signal. As a result, the second phase detector causes the kth clock signal to be phase locked to the digital data on the first data channel. In the embodiment described, the second phase detector supplies the selection signal to a second low pass filter 33. The second low pass filter averages the phase variation which is passed to the kth clock signal. The average phase correction rate can be calculated to provide selection of updates even in the absence of data transitions in the incoming data stream. Thus, a clock signal with a frequency offset from the reference clock signal may be generated. For example, constant variation, or precession, in the selected tap may be used to generate a clock signal with a greater or a lesser frequency than the reference clock signal.

The second multiplexer unit also generates a sampling signal 303. The sampling signal is provided as a clock input to clocked registers 139a-d, which are shown as receiving data signals. The sampling signal is a delayed version of the kth delay signal. In general, the kth delay signal provides a clock signal with edges approximately synchronized to the data transitions in the incoming data stream. In sampling the data stream, it is preferred to sample the incoming data stream about the center, variously defined, of the data eye. Thus, assuming that a signal

phase shifted half of a cycle from the kth delay signal provides an optimal sampling point the relative position of the zero delay selector and the [[nth]]Nth delay selector may be used to determine the appropriate tap for selection for the sampling signal.

In one embodiment, therefore, the difference between the [[nth]]Nth tap position and the zero tap position is divided by two and added (or subtracted depending on the position of the kth tap at any given moment) to the value of the kth tap position. The resulting value allows a selector to determine the tap for the sampling signal.